REMARKS

Claims 1-20 are pending in the application.

Claims 1-20 are rejected under 35 U.S.C. § 102(e).

Claim Rejections - 35 USC § 102

Claims 1-20 are rejected under 35 U.S.C. § 102(e) as being anticipated by Okayasu (U.S. Patent No. 6,157,200).

Applicant traverses this rejection.

Claim 1 recites,

"a plurality of control units, each control unit configured to electrically connect a corresponding comparator and driver unit to a pin of the semiconductor device in response to a control signal, wherein pins of the semiconductor device are divided into pin groups, each pin group having K number of pins, where K is an integer greater than 1."

Okayasu does not, however, teach or disclose the above-limitations of claim 1. Figs. 5, 10 and 12 clearly show a single pin P controlled by pin electronics 102A. In addition, col. 5, lines 9-12 state that a pattern signal is supplied "to one terminal P". Thus, Okayasu does not teach or disclose dividing pins of a DUT into pin groups, each group having one or more pins. Therefore, for at least this reason, claim 1 is not anticipated by Okayasu, and removal of the rejection is requested.

The applicant asserts that claims 2-7, which recite additional novel and non-obvious features, are also in condition for allowance.

Claim 8 recites,

"selecting pins from among a plurality of pins of the semiconductor device;

dividing the selected pins into a plurality of pin groups, each pin group comprising a desired plural number of pins." See, for example, the embodiment of applicant's Fig. 2 showing four-wide pin groups that connect control units 322_1...322_j to the DUT 40.

Okayasu does not, however, teach or disclose the above-limitations of claim 8. Figs. 5, 10 and 12 clearly show a single pin P controlled by pin electronics 102A. In addition, col. 5, lines 9-12 state that a pattern signal is supplied "to one terminal P". Thus, Okayasu does not teach or disclose selecting and dividing pins of a DUT into a plurality of pin groups. Therefore, for at least this reason, claim 8 is not anticipated by Okayasu, and removal of the rejection is requested.

The applicant asserts that claims 9-11, which recite additional novel and non-obvious features, are also in condition for allowance.

Claim 12 recites a pattern memory comprising an input memory and an output memory. Support for these limitations is, among other locations, on page 5, lines 16-18.

Okayasu does not, however, teach or disclose all of the limitations of claim 12. Figs. 1 and 4 clearly show a pattern generator 201 that does not store output signal patterns, as can be verified by following the data flow of the block diagrams of the figures. Also, col. 1, lines 24-25 state "*a pattern generator 201, from which test pattern data is output*" [emphasis added]. Thus, Okayasu does not teach or disclose a pattern memory comprising an input pattern memory and an output pattern memory. Therefore, for at least this reason, claim 12 is not anticipated by Okayasu, and removal of the rejection is requested.

The applicant asserts that claims 13-15, which recite additional novel and non-obvious features, are also in condition for allowance.

Claim 16 recites a semiconductor device having many pins using a test system having fewer pins. Support for these limitations is, among other locations, on page 4, lines 30-31 [*Each control unit...connects a corresponding one of the comparator and driver units...to two or more pins so that multiple pins share a comparator and driver unit.* (Emphasis added)].

Okayasu does not, however, teach or disclose all of the limitations of claim 16. Figs. 5, 10 and 12 clearly show a single pin P controlled by pin electronics 102A. In addition, col. 5, lines 9-12 state that a pattern signal is supplied "to one terminal P". In other words, Okayasu has a one-to-one correspondence of DUT pins to pins of the pin electronics 102A. Thus, Okayasu does not teach or disclose a method to choose one of several DUT pins all connected to a single comparator and driver unit. Therefore, for at least this reason, claim 16 is not anticipated by Okayasu, and removal of the rejection is requested.

The applicant asserts that claims 17-20, which recite additional novel and non-obvious features, are also in condition for allowance.

For the foregoing reasons, reconsideration and allowance of claims 1-20 of the application is solicited. The Examiner is encouraged to telephone the undersigned at (503) 222-3613 if it appears that an interview would be helpful in advancing the case.

Customer No. 20575

Respectfully submitted,

MARGER JOHNSON & McCOLLOM, P.C.

Joseph S. Makuch
Reg. No. 39,286

MARGER JOHNSON & McCOLLOM, P.C.
1030 SW Morrison Street
Portland, OR 97205
503-222-3613

I hereby certify that this correspondence is being transmitted to the U.S. Patent and Trademark Office via facsimile number (703) 872-9306 on January 20, 2005.

Stormi R. Davis